Application Note

Kodak KSC-1000 Programming Examples - KAF-16802 Image Sensor

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Revision 1.0

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INTRODUCTION

The KSC-1000 is a programmable CCD timing generator that is designed to interface with the entire family of Kodak Interline and Full Frame area array CCDs. The KSC-1000 uses traditional registers for defining the 13 pixel rate clocks, electronic shutter pulse generation, and general setup and control. Line Tables are used to define 6 outputs during the vertical clocking interval. Frame Tables are used to sequence the line table to create an image frame and to control portions of an imaging system. The KSC-1000 can be programmed to control image system timing or be slaved to an external controller.

This application note presents several examples of Line Table and Frame Table programming. The General Setup Register is also covered. The INTG_STRT functionality is not typically used in Full-Frame image sensor designs and therefore is not covered. The programming of the other General Purpose Registers is not covered in this application note, as the offsets, widths and polarity of the pixel rate clocks are dependent upon the application requirements and the clock driver design.

LINE TABLE EXAMPLES

I/O Mapping

The KSC-1000 line tables are used to define the states of the signals V1, V2, V3, V4, V5, and V6. These signals are used as inputs to a vertical clock driver circuit. It is assumed that a non-inverting driver circuit is used for the examples below. The I/O map for the examples is detailed in Table 1 below.

KSC-1000 Output	KAF-16802 Driver	Logic 1 Selection	Logic 0 Selection
V1	V1 Driver	High V1 Level	Low V1 Level
V2	V2 Driver	High V2 Level	Low V2 Level
V3	Not Used		
V4	Not Used		
V5	Not Used		
V6	Not Used		

Table 1 KSC-1000 toKAF-16802 Vertical Clock Driver Signal Map

Figure 1 is a copy of the line timing requirements from the KAF-16802 Device Performance Specification.

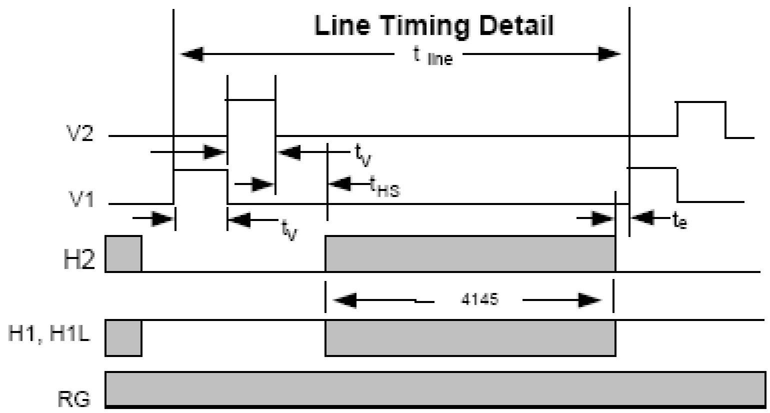

Figure 1 KAF-16802 Line Timing Requirements

Table 2 lists the Timing Requirements for the KAF-16802. A 20MHz pixel clock frequency is assumed for the line table examples that follow. This equates to 50nS pixel period. The value in the count field is the number of pixel clock cycles that are required to produce the desired time period. For example, 360 pixel clock periods of 50nS each are required to produce the 18uS T_{VW} time.

Timing Requirements

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
H1, H2 Clock Frequency	f_H		10	20	MHz	1, 2
V1, V2 Clock Frequency	f_V		25	50	kHz	1, 2
H1L, H1, H2 Rise, Fall Times	t_{Hr} , t_{Hf}	5		10	%	3, 8
V1, V2 Rise, Fall Times	t_{Vr} , t_{Vf}	5		10	%	3
V1 - V2 Cross-over	V_{VCR}	-1	0		V	
H1 - H2 Cross-over	V_{HCR}	30	50	70	%	4
Pixel Period (1 Count)	t_e	50	100		ns	2
H1, H2 Setup Time	t_{HS}	1	5		µs	
RG Clock Pulse Width	t_{RGw}	10	20		ns	5
RG Rise, Fall Times	t_{RGr} , t_{RGf}	5		10	%	3
V1, V2 Clock Pulse Width	t_{Vw}	15	18		µs	2, 7
H1L – VOUT Delay	t_{HV}		5		ns	
RG - VOUT Delay	t_{RV}		5		ns	
Readout Time	$t_{readout}$	983.5	1897		ms	7, 9
Integration Time	t_{int}					6, 7
Line Time	t_{line}	238.3	459.6		µs	7
Flush Time	t_{flush}	124	149		ms	

Notes:
1. 50% duty cycle values.
2. CTE will degrade above the nominal frequency.
3. Relative to the pulse width (based on 50% of high/low levels).
4. Relative to clock amplitude.
5. RG should be clocked continuously.
6. Integration time is user specified.
7. Longer times will degrade noise performance.
8. The maximum specification or 10nsec whichever is greater based on the frequency of the horizontal clocks.
9. $t_{readout} = t_{line} * 4128$ lines.

Table 2 KAF-16802 Timing Requirements

Line Table 0 – Readout Vertical Clocking

Table 3 is an example of a line table that implements the readout vertical clocking timing shown for Figure 1. The table uses the signal mappings described above. The line table address of 0 is an arbitrary selection. The frame table architecture permits random accessing of the line tables. The pixel clock frequency is assumed to be 20MHz, producing a 50nS pixel clock period.

Entry	Label	Value	Time	Comment
0	Count	360	18uS	360 50nS clock periods required for a 18uS period
0	HCLK_H	0		Set to 0, not last active entry in the line table
0	V6	0		Not Used
0	V5	0		Not Used
0	V4	0		Not Used
0	V3	0		Not Used
0	V2	0		V2 driver at low level
0	V1	1		V1 driver at high level
1	Count	360	18uS	360 50nS clock periods required for a 18uS period
1	HCLK_H	0		Set to 0, not last active entry in the line table
1	V6	0		Not Used
1	V5	0		Not Used
1	V4	0		Not Used
1	V3	0		Not Used
1	V2	1		V2 driver at high level
1	V1	0		V1 driver at low level
2	Count	20	1uS	20 50nS clock periods required for a 1uS period
2	HCLK_H	1		Set to 1, proceed to horizontal readout upon completion of line table
2	V6	0		Not Used
2	V5	0		Not Used
2	V4	0		Not Used
2	V3	0		Not Used
2	V2	0		V2 driver at low level
2	V1	0		V1 driver at low level

3	Count	0	0	All zero entry to indicate end of line table
3	HCLK_H	0		
3	V6	0		
3	V5	0		
3	V4	0		
3	V3	0		
3	V2	0		
3	V1	0		

Table 3 Line Table 0 Readout Vertical Clocking

To program this line table, the user initiates a write to register 9, the Line Table Access Register. The 8-bit line table address is programmed next. The address consists of an entry number followed by the table number. The 4 20 bit data entries complete the bit stream for this register.

The serial data is always written LSB first. The Line Table Address needs to written 1 time only if the auto-incrementing feature of the Line Table serial interface is used. The entries are programmed in ascending order starting at the entry number specified in the Line Table Address. Program execution from a line table always starts at entry 0. The bit streams for Line Table 0 (Table 3 above) are shown in the Table 4 below.

Register Address Label	**RNW**	**A0**	**A1**	**A2**	**A3**			
Register Address Bit Stream	0	1	0	0	1			
Line Table Address Label	**Entry 0**	**Address 0**						
Line Table Address Bit Stream	0000	0000						
Data Entry Label	**Count**	**HCLK_H**	**V6**	**V5**	**V4**	**V3**	**V2**	**V1**
Entry 0 Bit Stream	0001011010000	0	0	0	0	0	0	1
Entry 1 Bit Stream	0001011010000	0	0	0	0	0	1	0
Entry 2 Bit Stream	0010100000000	1	0	0	0	0	0	0
Entry 3 Bit Stream	0000000000000	0	0	0	0	0	0	0

Table 4 Line Table 0 Bit Stream

Line Table 1 – Power Up Flush Cycle

Figure 2 shows the timing required to flush the KAF-16802 upon power up.

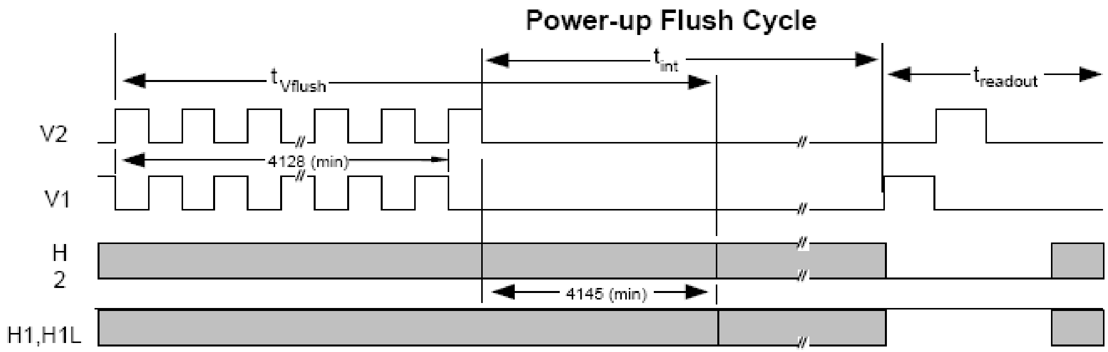

Figure 2 Power Up Flush Cycle

Table 5 is an example of a line table that shows the vertical clocking sequence shown in Figure 2. This line table is assigned to address 1.

Entry	Label	Value	Time	Comment
0	Count	300	15uS	300 50nS clock periods required for a 15uS period
0	HCLK_H	0		Set to 0, not last active entry in the line table
0	V6	0		Not Used
0	V5	0		Not Used
0	V4	0		Not Used
0	V3	0		Not Used
0	V2	0		V2 driver at low level
0	V1	1		V1 driver at high level
1	Count	300	15uS	300 50nS clock periods required for a 15uS period
1	HCLK_H	0		Set to 0, do not proceed to horizontal readout upon completion of line table
1	V6	0		Not Used
1	V5	0		Not Used
1	V4	0		Not Used
1	V3	0		Not Used
1	V2	1		V2 driver at high level
1	V1	1		V1 driver at low level
2	Count	0		All zero entry to indicate end of line table
2	HCLK_H	0		
2	V6	0		
2	V5	0		
2	V4	0		
2	V3	0		
2	V2	0		
2	V1	0		

Table 5 Line Table 1 Power Up Flush Cycle

The serial bit stream for Line Table 1 is shown in Table 6 below:

Register Address Label	RNW	A0	A1	A2	A3			
Register Address Bit Stream	0	1	0	0	1			
Line Table Address Label	**Entry 0**	**Address 1**						
Line Table Address Bit Stream	0000	1000						
Data Entry Label	**Count**	**HCLK_H**	**V6**	**V5**	**V4**	**V3**	**V2**	**V1**
Entry 0 Bit Stream	0011010010000	0	0	0	0	0	0	1
Entry 1 Bit Stream	0011010010000	0	0	0	0	0	1	0
Entry 2 Bit Stream	0000000000000	0	0	0	0	0	0	0

Table 6 Line Table 1 Bit Stream

Line Table 2 – Idle Vertical Clocks for 4145 Clocks

Table 7 is an example of a line table that holds the vertical clocks idle. In this case the vertical clocks are held idle for 4145 horizontal clock cycles to complete flushing of the horizontal CCD upon power up. This line table is assigned to address 2.

Entry	Label	Value	Time	Comment
0	Count	4145	207uS	4145 50nS clock periods required to complete flush cycle
0	HCLK_H	0		Set to 0, not last active entry in the line table
0	V6	0		Not Used
0	V5	0		Not Used
0	V4	0		Not Used
0	V3	0		Not Used
0	V2	0		V2 driver at low level
0	V1	0		V1 driver at low level
1	Count	0	0	All zero entry to indicate end of line table
1	HCLK_H	0		
1	V6	0		
1	V5	0		
1	V4	0		
1	V3	0		
1	V2	0		
1	V1	0		

Table 7 Line Table 2 Vertical Clocks Idle for 4145 Pixel Clocks

The serial bit stream for Line Table 2 is shown in Table 8 below

Register Address Label	RNW	A0	A1	A2	A3			
Register Address Bit Stream	0	1	0	0	1			
Line Table Address Label	**Entry 0**	**Address 2**						
Line Table Address Bit Stream	0000	0100						
Data Entry Label	**Count**	**HCLK_H**	**V6**	**V5**	**V4**	**V3**	**V2**	**V1**
Entry 0 Bit Stream	1000110000001	0	0	0	0	0	0	0
Entry 1 Bit Stream	0000000000000	0	0	0	0	0	0	0

Table 8 Line Table 2 Serial Bit Stream

Line Table 3 – Idle Vertical Clocks for 100uS Integration Tick

Table 9 implements a vertical clock idle period of 100uS. This time was arbitrarily chosen as the minimum integration time unit. Longer integration times can be achieved by repeatedly calling this line table.

Entry	Label	Value	Time	Comment
0	Count	2000	100uS	2000 50nS clock periods required for a 100uS period
0	HCLK_H	0		Set to 0, do not proceed to horizontal readout upon completion of line table
0	V6	0		Not Used
0	V5	0		Not Used
0	V4	0		Not Used
0	V3	0		Not Used
0	V2	0		V2 driver at low level
0	V1	0		V1 driver at low level
1	Count	0	0	All zero entry to indicate end of line table
1	HCLK_H	0		
1	V6	0		
1	V5	0		
1	V4	0		
1	V3	0		
1	V2	0		
1	V1	0		

Table 9 Line Table 3 Vertical Clocks Idle for 100uS

The serial bit stream for Line Table 3 is shown in Table 10 below:

Register Address Label	RNW	A0	A1	A2	A3			
Register Address Bit Stream	0	1	0	0	1			
Line Table Address Label	**Entry 0**	**Address 3**						
Line Table Address Bit Stream	0000	1100						
Data Entry Label	**Count**	**HCLK_H**	**V6**	**V5**	**V4**	**V3**	**V2**	**V1**
Entry 0 Bit Stream	0000101111100	0	0	0	0	0	0	0
Entry 1 Bit Stream	0000000000000	0	0	0	0	0	0	0

Table 10 Line Table 3 Serial Bit Stream

FRAME TABLE EXAMPLES

Frame Tables are used to link together a sequence of line tables. In the following example, Frame Table 0 is configured for a flush, integrate, and readout cycle. An idle state is entered at completion of the readout cycle. The VD signal is used to exit the idle state and start the flush, integrate, and readout cycle over again.

Frame Table 0

Entry 0 is an example of the ExLT command. This entry calls Line Table 1, which is used to generate vertical clocks for flushing. Setting the HCLK_V enable bit causes the horizontal clocks to run continuously during the vertical interval. All clamping is disabled in this entry. Frame Valid, Line Valid, and PBLK are disabled. No management of the Vertical Line Counter is necessary for any of the following entries, as the electronic shuttering functionality is not used

Label	Value	Comment
Check and Increment Line Counter	0	Do not increment Line Counter or compare with INTG_STRT Line Register
Clear Line Counter	0	Clear Line Counter
Force INTG_STRT	0	Do not force INTG_STRT
Horizontal Binning Factor	0	No Binning
HCLK_V Enable	1	Enable HCLKS during Vertical Interval
Line Valid Enable	0	Disable Line Valid
Frame Valid Enable	0	Disable Frame Valid
Video Amplifier Enable	0	Disable Video Amplifier
AFE Clock Enable	0	Disable AFE Clocks
CLPDM2 Enable	0	Disable Line Rate clamp
CLPDM1 Enable	0	Disable Frame Rate clamp
CLPOB2 Enable	0	Disable Line Rate clamp
CLPOB1 Enable	0	Disable Frame Rate clamp
PBLK Enable	0	Disable PBLK
PBLK Idle Val	1	PBLK active low
Flag	0	
Count	4128	Execute Line Table 1 4128X, proceed to next entry when finished
Address 2:0	1	
Address 3	0	

Table 11 Frame Table 0, Entry 0

Entry 1 is another example of the ExLT command. This entry calls Line Table 2, which keeps the vertical clocks in their idle state while the horizontal CCD is flushed out. All of the clamps are disabled. Frame Valid and Line Valid, and PBLK are disabled.

Label	Value	Comment
Check and Increment Line Counter	0	Do not increment Line Counter and compare with INTG_STRT Line Register
Clear Line Counter	0	Do not clear Line Counter
Force INTG_STRT	0	Do not force INTG_STRT
Horizontal Binning Factor	0	No Binning
HCLK_V Enable	1	Enable HCLKS during Vertical Interval
Line Valid Enable	0	Disable Line Valid
Frame Valid Enable	0	Disable Frame Valid
Video Amplifier Enable	0	Disable Video Amplifier
AFE Clock Enable	0	Disable AFE Clocks
CLPDM2 Enable	0	Disable Line Rate clamp
CLPDM1 Enable	0	Disable Frame Rate clamp
CLPOB2 Enable	0	Disable Line Rate clamp
CLPOB1 Enable	0	Disable Frame Rate clamp
PBLK Enable	0	Disable PBLK
PBLK Idle Val	1	PBLK active low
Flag	0	
Count	1	Execute Line Table 2 1x, proceed to next entry when finished
Address 2:0	2	
Address 3	0	

Table 12 Frame Table 0, Entry 1

Entry 2 implements the ExLTNVD command. This entry calls Line Table 3. This table holds the vertical clocks in their idle state for a 100us interval. This 100uS interval is the integration time tick. An external controller controls the integration time by generating a VD signal to exit this entry. All of the clamps are disabled. Frame Valid and Line Valid, and PBLK are disabled.

Label	Value	Comment
Check and Increment Line Counter	0	Do not increment Line Counter and compare with INTG_STRT Line Register
Clear Line Counter	0	Do not clear Line Counter
Force INTG_STRT	0	Do not force INTG_STRT
Horizontal Binning Factor	0	No Binning
HCLK_V Enable	1	Enable HCLKS during Vertical Interval
Line Valid Enable	0	Disable Line Valid
Frame Valid Enable	0	Disable Frame Valid
Video Amplifier Enable	0	Disable Video Amplifier
AFE Clock Enable	0	Disable AFE Clocks
CLPDM2 Enable	0	Disable Line Rate clamp
CLPDM1 Enable	0	Disable Frame Rate clamp
CLPOB2 Enable	0	Disable Line Rate clamp
CLPOB1 Enable	0	Disable Frame Rate clamp
PBLK Enable	0	Disable PBLK
PBLK Idle Val	1	PBLK active low
Flag	1	
Count	0	Execute Line Table 3 repeatedly until a VD event is detected.
Address 2:0	3	
Address 3	0	

Table 13 Frame Table 0, Entry 2

Entry 3 implements ExLT command again. This entry starts the image readout. This entry calls line table 0 once to clock out the first dark line. Horizontal readout is enabled after completion of this line table. Line Valid, Frame Valid, and PBLK are disabled. All clamping is disabled.

Label	Value	Comment
Check and Increment Line Counter	0	Do not increment Line Counter and compare with INTG_STRT Line Register
Clear Line Counter	0	Do not clear Line Counter
Force INTG_STRT	0	Do not force INTG_STRT
Horizontal Binning Factor	0	No Binning
HCLK_V Enable	0	Do not enable HCLKS during Vertical Interval
Line Valid Enable	0	Disable Line Valid
Frame Valid Enable	0	Disable Frame Valid
Video Amplifier Enable	1	Enable Video Amplifier
AFE Clock Enable	1	Enable AFE Clocks
CLPDM2 Enable	0	Disable Line Rate clamp
CLPDM1 Enable	0	Disable Frame Rate clamp
CLPOB2 Enable	0	Disable Line Rate clamp
CLPOB1 Enable	0	Disable Frame Rate clamp
PBLK Enable	0	Disable PBLK
PBLK Idle Val	1	PBLK active low
Flag	0	
Count	1	Execute Line Table 0 1x, proceed to next entry when finished
Address 2:0	0	
Address 3	0	

Table 14 Frame Table 0, Entry 3

Entry 4 is another implementation of the ExLT command. In this case 18 dark rows are read out with Frame Rate clamping enabled. Frame Valid, Line Valid, PBLK, and Line Rate Clamping are disabled.

Label	Value	Comment
Check and Increment Line Counter	0	Do not increment Line Counter and compare with INTG_STRT Line Register
Clear Line Counter	0	Do not clear Line Counter
Force INTG_STRT	0	Do not force INTG_STRT
Horizontal Binning Factor	0	No Binning
HCLK_V Enable	0	Do not enable HCLKS during Vertical Interval
Line Valid Enable	0	Disable Line Valid
Frame Valid Enable	0	Disable Frame Valid
Video Amplifier Enable	1	Enable Video Amplifier
AFE Clock Enable	1	Enable AFE Clocks
CLPDM2 Enable	0	Disable Line Rate clamp
CLPDM1 Enable	1	Enable Frame Rate clamp
CLPOB2 Enable	0	Disable Line Rate clamp
CLPOB1 Enable	1	Enable Frame Rate clamp
PBLK Enable	0	Disable PBLK
PBLK Idle Val	1	PBLK active low
Flag	0	
Count	18	Execute Line Table 0 18x, proceed to next entry when finished
Address 2:0	0	
Address 3	0	

Table 15 Frame Table 0, Entry 4

Entry 5 is another example of the ExLT command. This entry reads out the remaining dark line at the top of the image along with 9 active buffer lines. Line Rate clamping is enabled. Frame Rate clamping, Line Valid, Frame Valid, and PBLK are all disabled.

Label	Value	Comment
Check and Increment Line Counter	0	Do not increment Line Counter or compare with INTG_STRT Line Register
Clear Line Counter	0	Do not clear Line Counter
Force INTG_STRT	0	Do not force INTG_STRT
Horizontal Binning Factor	0	No Binning
HCLK_V Enable	0	Do not enable HCLKS during Vertical Interval
Line Valid Enable	0	Do not Enable Line Valid
Frame Valid Enable	0	Do not enable Frame Valid
Video Amplifier Enable	1	Enable Video Amplifier
AFE Clock Enable	1	Enable AFE Clocks
CLPDM2 Enable	1	Enable Line Rate clamp
CLPDM1 Enable	0	Disable Frame Rate clamp
CLPOB2 Enable	1	Enable Line Rate clamp
CLPOB1 Enable	0	Disable Frame Rate clamp
PBLK Enable	0	Set PBLK high
PBLK Idle Val	1	PBLK active low
Flag	0	
Count	10	Execute Line Table 0 10x, proceed to next entry when finished
Address 2:0	0	
Address 3	0	

Table 16 Frame Table 0, Entry 5

Entry 6 uses the ExLT again. This entry is used to read out 4080 active image lines. Line Rate clamping, Frame Valid, and Line Valid are enabled. Frame Rate clamping, and PBLK are disabled.

Label	Value	Comment
Check and Increment Line Counter	0	Do not increment Line Counter or compare with INTG_STRT Line Register
Clear Line Counter	0	Do not Clear Line Counter
Force INTG_STRT	0	Do not force INTG_STRT
Horizontal Binning Factor	0	No Binning
HCLK_V Enable	0	Do not enable HCLKS during Vertical Interval
Line Valid Enable	1	Enable Line Valid
Frame Valid Enable	1	Enable Frame Valid
Video Amplifier Enable	1	Enable Video Amplifier
AFE Clock Enable	1	Enable AFE Clocks
CLPDM2 Enable	1	Enable Line Rate clamp
CLPDM1 Enable	0	Disable Frame Rate clamp
CLPOB2 Enable	1	Enable Line Rate clamp
CLPOB1 Enable	0	Disable Frame Rate clamp
PBLK Enable	0	Disable PBLK
PBLK Idle Val	1	PBLK active low
Flag	0	
Count	4080	Execute Line Table 0 4080x, proceed to next entry when finished
Address 2:0	0	
Address 3	0	

Table 17 Frame Table 0, Entry 6

Entry 7 is another example of the ExLT command. This entry reads out 9 active buffer lines, 9 dark lines, and 1 active CTE monitor line at the bottom of the image. Line Rate clamping is enabled. Frame Rate clamping, Line Valid, Frame Valid, and PBLK are all disabled.

Label	Value	Comment
Check and Increment Line Counter	0	Do not increment Line Counter or compare with INTG_STRT Line Register
Clear Line Counter	0	Do not clear Line Counter
Force INTG_STRT	0	Do not force INTG_STRT
Horizontal Binning Factor	0	No Binning
HCLK_V Enable	0	Do not enable HCLKS during Vertical Interval
Line Valid Enable	0	Do not Enable Line Valid
Frame Valid Enable	0	Do not enable Frame Valid
Video Amplifier Enable	1	Enable Video Amplifier
AFE Clock Enable	1	Enable AFE Clocks
CLPDM2 Enable	1	Enable Line Rate clamp
CLPDM1 Enable	0	Disable Frame Rate clamp
CLPOB2 Enable	1	Enable Line Rate clamp
CLPOB1 Enable	0	Disable Frame Rate clamp
PBLK Enable	0	Set PBLK high
PBLK Idle Val	1	PBLK active low
Flag	0	
Count	19	Execute Line Table 0 19x, proceed to next entry when finished
Address 2:0	0	
Address 3	0	

Table 18 Frame Table 0, Entry 7

Entry 8 implements the ExLTNVD command. This entry calls Line Table 3. This table holds the vertical clocks in their idle state indefinitely until a VD event is sensed. All of the clamps are disabled. Frame Valid and Line Valid, and PBLK are disabled.

Label	Value	Comment
Check and Increment Line Counter	0	Do not increment Line Counter and compare with INTG_STRT Line Register
Clear Line Counter	0	Do not clear Line Counter
Force INTG_STRT	0	Do not force INTG_STRT
Horizontal Binning Factor	0	No Binning
HCLK_V Enable	0	Disable HCLKS during Vertical Interval
Line Valid Enable	0	Disable Line Valid
Frame Valid Enable	0	Disable Frame Valid
Video Amplifier Enable	0	Disable Video Amplifier
AFE Clock Enable	0	Disable AFE Clocks
CLPDM2 Enable	0	Disable Line Rate clamp
CLPDM1 Enable	0	Disable Frame Rate clamp
CLPOB2 Enable	0	Disable Line Rate clamp
CLPOB1 Enable	0	Disable Frame Rate clamp
PBLK Enable	0	Disable PBLK
PBLK Idle Val	1	PBLK active low
Flag	1	
Count	0	Execute Line Table 3 repeatedly until a VD event is detected.
Address 2:0	3	
Address 3	0	

Table 19 Frame Table 0, Entry 8

Entry 9 implements the JmpFT command. In this case, control is passed back to Entry 0 of this Frame Table. The state of the control bits does not matter for the jump instructions.

Label	Value	Comment
Check and Increment Line Counter	0	Do not increment Line Counter and compare with INTG_STRT Line Register
Clear Line Counter	0	Do not clear Line Counter
Force INTG_STRT	0	Do not force INTG_STRT
Horizontal Binning Factor	0	No Binning
HCLK_V Enable	0	Disable HCLKS during Vertical Interval
Line Valid Enable	0	Disable Line Valid
Frame Valid Enable	0	Disable Frame Valid
Video Amplifier Enable	0	Disable Video Amplifier
AFE Clock Enable	0	Disable AFE Clocks
CLPDM2 Enable	0	Disable Line Rate clamp
CLPDM1 Enable	0	Disable Frame Rate clamp
CLPOB2 Enable	0	Disable Line Rate clamp
CLPOB1 Enable	0	Disable Frame Rate clamp
PBLK Enable	0	Disable PBLK
PBLK Idle Val	1	PBLK active low
Flag	0	
Count	0	Jump to Frame Table 0, Entry 0
Address 2:0	0	
Address 3	0	

Table 20 Frame Table 0, Entry 9

To program Frame Table 0, the user initiates a write to register 8, the Frame Table Access Register. The 7-bit frame table address is programmed next. The address consists of an entry number followed by the table number. The 10 34 bit data entries complete the bit stream for this register.

The serial data is always written LSB first. The Frame Table Address needs to written 1 time only if the auto-incrementing feature of the Line Table serial interface is used. The entries are programmed in ascending order starting at the entry number specified in the Line Table Address. Program execution from a frame table always starts at entry 0. The bit streams for Frame Table 0 are shown in the Table 21 below.

Some of the individual control bits have been grouped in the table below. The INTG_STRT Cntl field consists of the Check and Increment Line Counter Bit (LSB), followed by Clear Line Counter Bit and the Force INTG_START bit in that order. The H Bin field consists of 2 bits. The Enables field consists of the HCLK_V Enable bit (LSB) followed by the Line Valid Enable bit, the Frame Valid Enable bit, the Video Amplifier Enable bit, the AFE Clock Enable bit, the CLPDM2 Enable bit, the CLPDM1 Enable bit, the CLPOB2 Enable bit, the CLPOB1 Enable bit, and the PBLK enable bit in that order. The count field contains 13 bits.

Register Address Label	**RNW**	**A0**	**A1**	**A2**	**A3**			
Register Address Bit Stream	0	0	0	0	1			
Line Table Address Label	**Entry 0**	**Addr 0**						
Line Table Address Bit Stream	0000	000						
Data Entry Label	**INTG_STRT Cntl**	**H Bin**	**Enables**	**PBLK Idle**	**Flag**	**Count**	**A0:2**	**A3**
Entry 0 Bit Stream	000	00	1000000000	1	0	0000010000001	100	0
Entry 1 Bit Stream	000	00	1000000000	1	0	1000000000000	010	0
Entry 2 Bit Stream	000	00	1000000000	1	1	0000000000000	110	0
Entry 3 Bit Stream	000	00	0001100000	1	0	1000000000000	000	0
Entry 4 Bit Stream	000	00	0001101010	1	0	0100100000000	000	0
Entry 5 Bit Stream	000	00	0001110100	1	0	0101000000000	000	0
Entry 6 Bit Stream	000	00	0111110100	1	0	0000111111110	000	0
Entry 7 Bit Stream	000	00	0001110100	1	0	1100100000000	000	0
Entry 8 Bit Stream	000	00	0000000000	1	1	0000000000000	110	0
Entry 9 Bit Stream	000	00	0000000000	1	0	0000000000000	000	0

Table 21 Frame Table 0 Serial Bit Stream

GENERAL PURPOSE REGISTERS

There are 8 General Purpose Registers. The functionality of these registers are detailed in the KSC-1000 Device Performance Specification. The programming of the General Setup Register is described below.

General Setup Register

The values programmed in the General Setup Register are application dependent. For purposes of the discussion below, the following assumptions are made:

1. There is no over clocking of the horizontal shift register
2. It is desired to store only the active pixels
3. Line rate clamping occurs on the leading dark pixels
4. The CLPDM and CLPOB signals start and stop at the same pixel locations

The value programmed in the Pixels Per Line field is dependent upon the mode of image sensor operation. A value of 4145 is required to read out the entire horizontal CCD.

The Line Valid signal is typically used as a sync signal by an external framestore. The Line Valid Pixel Start field is programmed to a value of 44. This causes the 14 leading dummy pixels, the 20 leading dark pixels, 1 leading CTE Monitor pixel, and the 9 leading active buffer pixels to be discarded by the framestore. The Line Valid Pixel End field is programmed to a value of 4124. This will discard the 9 trailing active buffer pixels, 9 trailing dark pixels, 1 trailing CTE Monitor pixel and 2 trailing dummy pixels.

CLPOB_1 and CLPDM_1 are used for frame rate clamping. A value of 17 is programmed to the CLPDM_1 Pixel Start and CLPOB_1 Pixel Start fields. The CLPOB_1 Pixel End and CLPDM_1 Pixel End fields are programmed to a value of 4140. These selections allow clamping on the entire dark row with the exception of 2 pixels on either edge.

CLPOB_2 and CLPDM_2 are used for line rate clamping. A value of 17 is programmed to the CLPDM_2 Pixel Start and CLPOB_2 Pixel Start fields. The CLPOB_2 Pixel End and CLPDM_2 Pixel End fields are programmed to a value of 33. These selections allow clamping on the leading dark pixels with the exception of the 2 edge pixels.

PBLK is typically used to provide a blanking signal during the vertical clocking interval. For this application, the PBLK Pixel Start field is programmed the value in the Pixels Per Line field. The PBLK Pixel End field is programmed to a value of 0.

There are 14 enable bits for the all of the pixel clock rate outputs. For this example, the following assumptions regarding the pixel rate output clocks are made. H1, H2, and H3 are used for the horizontal clocks. SH1, SH2, DATACLK1 are used to drive the AFE chip. DATACLK2 is used to clock image data into an external image memory.

There are 13 24mA enable bits for all of the pixel rate outputs with the exception of PIXCLK. The 24mA drive selection provides faster rise and fall times. For this example, it is assumed that the 24mA drive is not used.

Finally, there are 4 bits to select the proper DLL for the desired pixel clock frequency. DLL 8 is chosen for the 20MHz pixel clock frequency.

The bit stream for Register 1 is shown in Table 22 below.

Label	Bit Field Width	Data	Bit Stream
Register Address	5	2	01000
Pixels Per Line	13	4145	1000110000001
Line Valid Pixel Start	13	44	0011010000000
Line Valid Pixel Quadrature Start	2	0	00
Line Valid Pixel End	13	4124	0011100000001
CLPOB1_Pix_Start	13	17	1000100000000
CLPOB1_Pix_End	13	4140	0011010000001
CLPOB2_Pix_Start	13	17	1000100000000
CLPOB2_Pix_End	13	33	1000010000000
CLPDM1_Pix_Start	13	17	1000100000000
CLPDM1_Pix_End	13	4140	0011010000001
CLPDM2_Pix_Start	13	17	1000100000000
CLPDM2_Pix_End	13	33	1000010000000
PBLK_Pix_Start	13	4145	1000110000001
PBLK_Pix_End	13	0	0000000000000
Pixel Rate Clock Enable Bits	14		10001011011110
Pixel Rate Clock 24mA Drive Enable Bits	13		0000000000000
DLL Select Bits	4	8	0001

Table 22 Register 1 Serial Bit Stream

REVISION CHANGES

Revision Number	Description of Changes
1.0	Initial release

Table 23 Revision History